REMARKS

Drawings

Applicant submits a revised FIG. 2 labeled as suggested by the Examiner.

Claim amendments

Applicant amends claim 21 to recite providing a first metallization plane rather than a first substructure plane. Amended claim 21 thus conforms more closely to the specification.[1] Applicant also amends claim 21 to recite providing the liner layer on the intermediate dielectric. This is consistent with the configuration shown in FIG. 1H of the application.

Section 102 rejection based on *Usami*

As best understood, the Examiner considers the liner layer recited in claim 21 to correspond to the "third inter-level isolation film **17**" shown in FIG. 4 of *Usami*.[2] This isolation film **17** has a section of reduced thickness defining a groove **13** between two interconnects **8**.

In response, Applicant draws attention to claim 21's recitation of

> *"interrupting said liner layer beween said first interconnect and said second interconnect, thereby forming an interspace between said first and second interconnects."*

There is no teaching in *Usami* that meets this claim limitation. As is apparent from FIG. 4, the third inter-level isolation film **17** extends across the groove **13** without interruption. Accordingly, *Usami* fails to teach or suggest interrupting a liner layer as recited in claim 21.

Claims 22-27 include all the limitations of claim 21. Hence, these claims are allowable for at least the same reasons that claim 21 is allowable.

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[1] See application between page 4, line 37 and page 5, line 1 ("As illustrated in figure 1a, first of all the first metallization layer M1 is deposited on the semiconductor substrate 1 and patterned.")
[2] *Usami*, U.S. Patent No. 6,498,398

Section 102 rejection based on *Yamaha*

The Si atoms at an Si interface often have an unfilled valence bond. These dangling valence bonds contribute to a high interface state density, which in turn results in slow switching speeds in transistors. In some cases, moisture-related species fill these valence bonds during final annealing.[3]

Because of its low contact-resistance, it is desirable to contact a Si layer with a Ti layer. Unfortunately, Ti has a tendency to compete for the same moisture-related species that would otherwise fill the dangling valence bonds.[4]

To suppress this competition, *Yamaha* provides a blocking film **15** between the Ti layers 16, 17, 19 and the first intermediate dielectric layer **14**.[5] As best understood, the Examiner considers this blocking film **15** to correspond to the liner layer recited in claim 21. To enable these moisture-related species to pass between the dielectric layers **18** and the first intermediate dielectric **14**, *Yamaha* provides openings in the blocking film **15**.[6] The Examiner appears to consider the making of these openings to correspond to the step of interrupting the liner layer in claim 21.

Yamaha lacks any teaching of "providing a first metallization plane" as recited in claim 21. In *Yamaha*'s FIG. 1I, the wiring layers are above non-metallic materials. As a result, the configuration of the liner layer does not significantly alter capacitative coupling between the wiring layer **19** and either of the two wiring layers **16** and **17**.

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[3] *Yamaha*, col. 5, lines 15-19 ("The inventors now consider that moisture related species (H_2O, OH^-, H^+) in the insulating film 18 diffuse to the Si/SiO_2 interface during the final annealing process and are terminated in the form of (Si≡Si-H, Si≡Si-OH)").

[4] *Yamaha*, col. 5, lines 20-24 ("If a Ti layer absorbing and storing moisture related species (H_2O, OH^-, H^+) is formed just above a transistor, the concentration of moisture related species in lowered near at the transistor, and the interface state density cannot be lowered").

[5] *Yamaha*, col. 5, lines 40-44 ("For these facts, it is desired to use a Ti layer while blocking the function of Ti layer of adsorbing and absorbing diffusion species such as moisture related species above the gate insulating film. This impervious function can be realized by inserting a silicon nitride film between the Ti layer and an underlying layer.")

[6] Yamaha, col. 5, lines 44-48 ("In order not to block the diffusion of moisture related species from the upper level layer, an opening or openings are formed in the silicon nitride film. This can be achieved by patterning the silicon nitride film together with the Ti layer").

In contrast, FIG. 1H of the specification shows first and second metallization planes **M1**, **M2** forming what amounts to two adjacent parallel plate capacitors. Applicant has discovered that an interruption in the liner layer **L** greatly reduces capacitative coupling between the two interconnects **LBA** and **LBB**. This is neither taught nor suggested by *Yamaha*.

Claims 22-27 include all the limitations of claim 21. Hence, these claims are allowable for at least the same reasons that claim 21 is allowable.

Section 103 rejection of claim 25

The Examiner suggests that claim 25 is rendered obvious by *Yamaha's* teaching that other materials that block diffusion of moisture-related species can be used in place of SiN.

Applicant notes that the third inter-level isolation film of *Usami* is not intended to block diffusion of moisture-related species. It is unclear what motivation exists to make that layer out of a material having a property unrelated to the function of that layer.

Accordingly, Applicant submits there is no motivation to combined the teaching of *Yamaha* and *Usami* as suggested by the Examiner.